This week, I complete the test of the uart\_rxd module and uart\_rxd\_rxd\_if module. I think they are a little more complex than the uart\_txd and uart\_txd\_if. In the higher level, I think I am lack of thoughts about how to test the top module. Especially I still don’t know how to test the module when the configuration varies. I think there are mainly two reasons. One is I don’t know the knowledge of verification. So I plan to study the systemverilog verification. The other reason is I can’t understand the detail of the uart module such as fifo. So I plan to try to write a fifo next week.